OCTERA Corporation

Verification Environment

Version 3.0, November 2011

Introduction

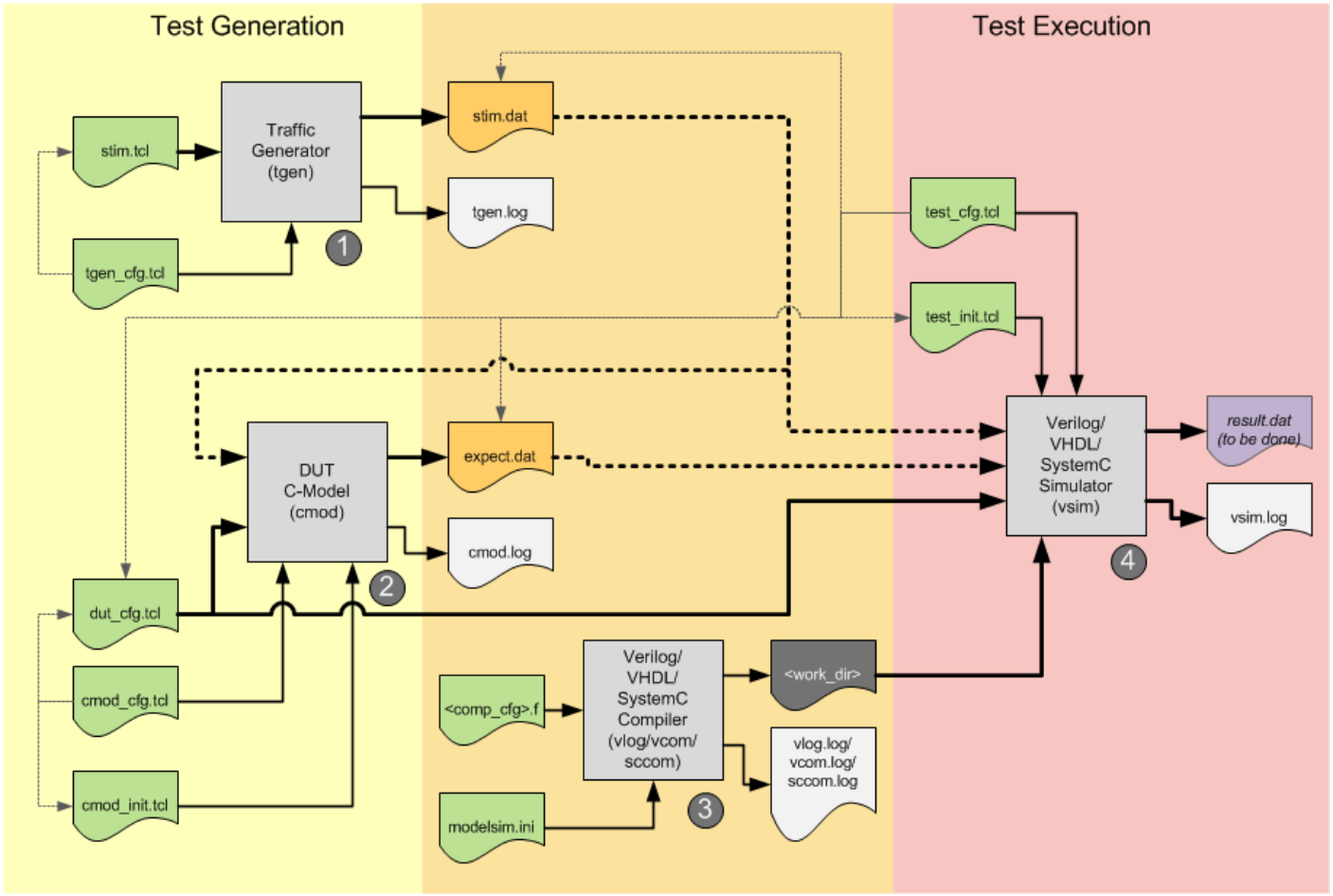
The Octera Verification Environment is a collection of C applications, scripts, and test benches that work together to provide a powerful and flexible verification environment for Networking FPGA designs.

The tool flow consists of scripted traffic generation, C modeling of the FPGA design and execution of a system level RTL simulation (VHDL and/or Verilog) using the generated traffic, the modeled results and full featured scriptable bus functional models for the interfaces.

Features

Traffic Generation

- **Fully scriptable collection of powerful, integrated traffic generation functions.**
- **Histogram based packet length generation allows for generation of any packet size profile.**
- **Flexible packet field definition. Fields can be fixed, generated from pools of values, or read from files.**
- **Inserts a unique 16-bit packet ID in each packet (location selectable) for packet identification during modeling and simulation.**
- **Generates L2, L3, and Custom packets.**
- **Integrated Checksum and CRC calculation.**



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C Modeling

- C Model is developed in C++. It consists of a project that can be built from a collection of classes, some of which are customized for the design under test.
- Tcl script interface for user host interface modeling, parameter setting and control of other model features
- Database class reads traffic files generated by the traffic generator, and writes modeled output traffic files. It allows packets to be selected from the input database in any order, and written to the output database in any order. It allows for bandwidth expansion and for changes in the number of packets generated.
- Passes packet data and parsed field information to modeling class (customized by the user), and accepts similarly formatted output packets.
- Provides messaging class for user model logging and message generation.

Bus Function Models (BFMs)

- BFMs are integrated by Octera for custom applications. A Tcl script interface is provided for host interface functions (compatible with the C model), BFM parameterization and simulation flow.
- Packet database class includes packet identification and checking functions.
- BFM classes for XAUI, XGMII, SPI4, PCI, Avalon-MM and Avalon-ST are available.
- BFMs interface at either the pins of the device or at a parallel internal interface. This approach lets the engineer choose a faster simulation run for debug or a full coverage simulation for final test.
- Detailed simulation logging with time stamping is provided.

Scripted Test Execution (gosim.pl)

- The Gosim environment is a Perl script that ties everything together.
- Allows for easy selection of different simulation tool versions.
- Allows running of tests in GUI or batch mode.
- Automatically runs the traffic generator and C Model, compiles the RTL design and runs the simulation.
- Manages lists of tests for full design verification and regression testing.
- Manages simulation options such as logging of simulation results.
- Provides a summary of test results and a final PASS/FAIL indication after the regression run completes.

Customization

- Traffic Generation
- C Modeling
- Simulation / BFM scripts
- Design compilation scripts
- Regression test lists
- Custom BFMs (if required.)

Deliverables

- Traffic Generator executable for Windows and RedHat / CentOS Linux.
- C Model source code, Microsoft Visual C++ Project, and Linux build scripts.
- Customized (or standard, if available) set of integrated BFMs.
- Gosim Perl script.
- Example directory structure.
- Example loopback design for demonstration purposes.
- User documentation.

Product code: OCT-VER

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