OCTERA Corporation

DDRx SDRAM Memory Backup

Version 3.0, November 2011

Introduction

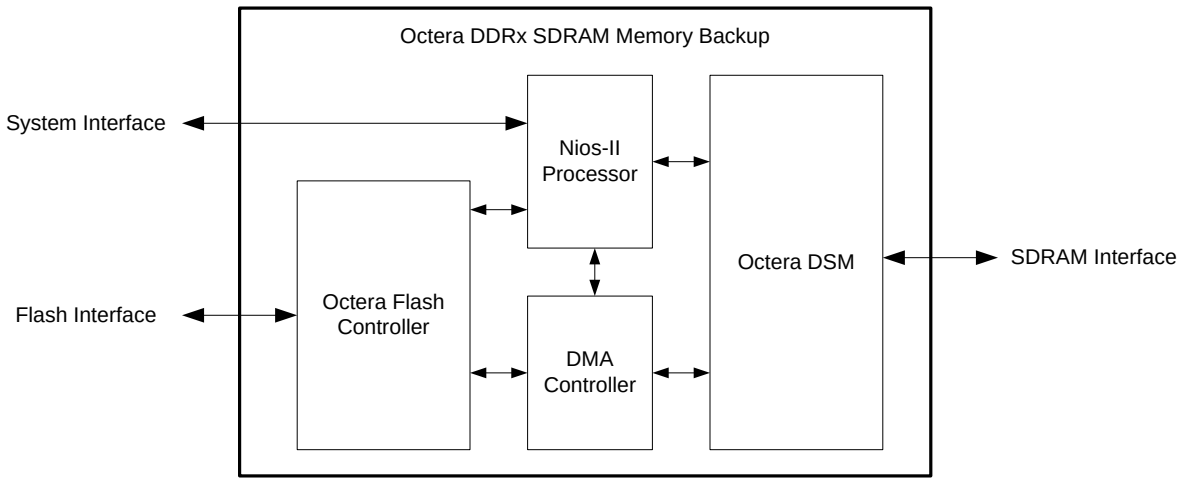
Traditionally, great lengths are taken to prevent power loss to a server. Sometimes it cannot be avoided. Restoring the server back up to its pre-powerdown state as quickly as possible is often a key feature of the server.

Octera has created custom blocks that will facilitate the transfer of data from DDR1/2/3 SDRAM memory to a non-volatile memory (i.e. flash) on a loss of power and then restore the data to SDRAM memory once power has been restored. An Altera Nios-II processor is used to communicate with the system and to initiate and monitor the backup and restore operations.

This solution targets the low-cost Cyclone family and has been successfully implemented in the smallest packages available.

Features

- **Minimal hardware requirements**
- **Maintains maximum data bandwidth during memory read and write operations**
- **Supports x8, x16 and x24 configurations of DDR1/2/3 SDRAM devices**
- **Supports up to 4GB of SDRAM memory (32-bit address)**
- **Blocks can be configured or customized for many unique applications.**



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Implementation Summary

Core Specifics		
Any Altera Family		
Speed Grade		
All		
Example Resource Utilization		
	Cyclone III *(16-bit DQ)*	***Cyclone IV*** *(24-bit DQ)*
LEs	14,802	25,791
Registers	8,688	14,729
RAM	55 M9Ks	102 M9Ks
PLLs	3	3
Pins	149	178
Supported Design Tools		
Altera	Quartus II 9.1SP2 or later	

Deliverables

- **Encrypted source code of custom hw blocks**
- **SOPC Builder generated output files**
- **Firmware**
- **Scripted verification environment**
- **DDR3 Bus Functional Models**

Product codes: OCT-DDR-BKUP

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