OCTERA Corporation

BCH Core

Version 1.1, January 2014

Introduction

The Octera BCH core consists of an encoder and decoder. The decoder implements the standard steps of calculating the syndromes followed by calculating the error location polynomial using Galois Field mathematics in hardware. The final correction uses a method that is more readily pipelined than the common Chien search.

Both the encoder and decoder are pipelined so messages can immediately follow each other, with the following limitations:

- **The input to the encoder must have a gap between messages long enough to permit the added ECC symbols to be inserted on the output.**
- **If only two buffers are used in the decoder to save resources, then in some cases an additional gap must be inserted between messages. This only happens with short messages combined with a high error correction capability, which is not common in practical applications.**

Features

The following features are limited only by the FPGA resources allocated to the BCH core and the needed clock rate:

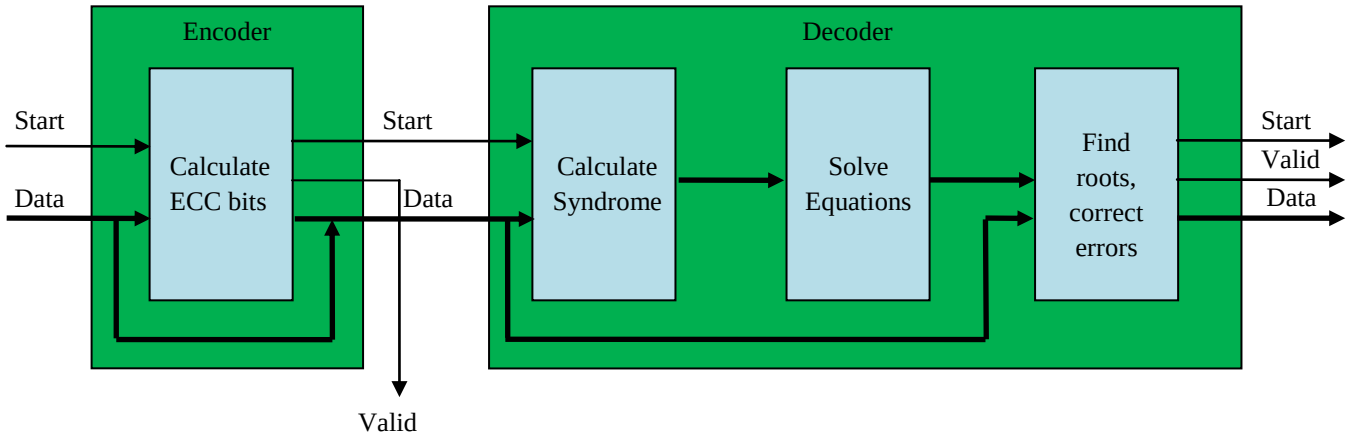
- **Can be provided to correct any requested # of errors providing the message length permits it**
- **Any Galois field order M**
- **Any primitive polynomial**
- **Any generator polynomial**
- **Any symbol width**

Customization

Octera can customize a BCH encoder or decoder for any legal combination of message length, symbol width, # of correctable errors, primitive polynomial (decoder), generator polynomial (encoder), Galois field order and number of buffers (decoder).

Deliverables

- **Encrypted source code**
- **Fully synthesized FPGA**



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Message Length (Symbols)	Correctable Errors (bits)	Symbol Width (bits)	Galois Field Order M	ECC (bits)	ECC Overhead (percent)	FPGA type	Encoder			Decoder		
							ALMs	Frequency (MHz)	Mbps	ALMs	Frequency (MHz)	Mbps
Effect of varying # of correctable errors, short message:												
250	1	1	8	8	3.2%	Stratix V C2	31	500	500	447	235	235
250	4	1	8	32	12.8%	Stratix V C2	42	500	500	1035	190	190
250	8	1	8	64	25.6%	Stratix V C2	58	500	500	1885	200	200
Effect of varying # of correctable errors, long message:												
1000	1	8	13	13	0.2%	Stratix V C2	46	500	4000	3587	150	1200
1000	4	8	13	52	0.7%	Stratix V C2	80	475	3800	6973	125	1000
971	32	8	13	416	5.4%	Stratix V C2	260	425	3400	40890	100	800
Effect of varying message length:												
250	4	8	11	44	2.2%	Stratix V C2	82	500	4000	3812	150	1200
500	4	8	12	48	1.2%	Stratix V C2	86	475	3800	5314	140	1120
1000	4	8	13	52	0.7%	Stratix V C2	80	475	3800	6973	125	1000
Effect of varying symbol width:												
2000	4	1	11	44	2.2%	Stratix V C2	47	500	500	1668	160	160
250	4	8	11	44	2.2%	Stratix V C2	82	500	4000	3812	160	1280
125	4	16	11	44	2.2%	Stratix V C2	116	500	8000	6320	160	2560
Effect of varying FPGA type:												
250	4	8	11	44	2.2%	Cyclone V C6	117	240	1920	3868	90	720
250	4	8	11	44	2.2%	Arria V C4	120	275	2200	3855	100	800
250	4	8	11	44	2.2%	Stratix V C2	82	500	4000	3812	150	1200
250	4	8	11	44	2.2%	Arria 10 I2	63	550	4400	3806	190	1520

Product code: OCT-BCH

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