OCTERA Corporation

PowerPC405

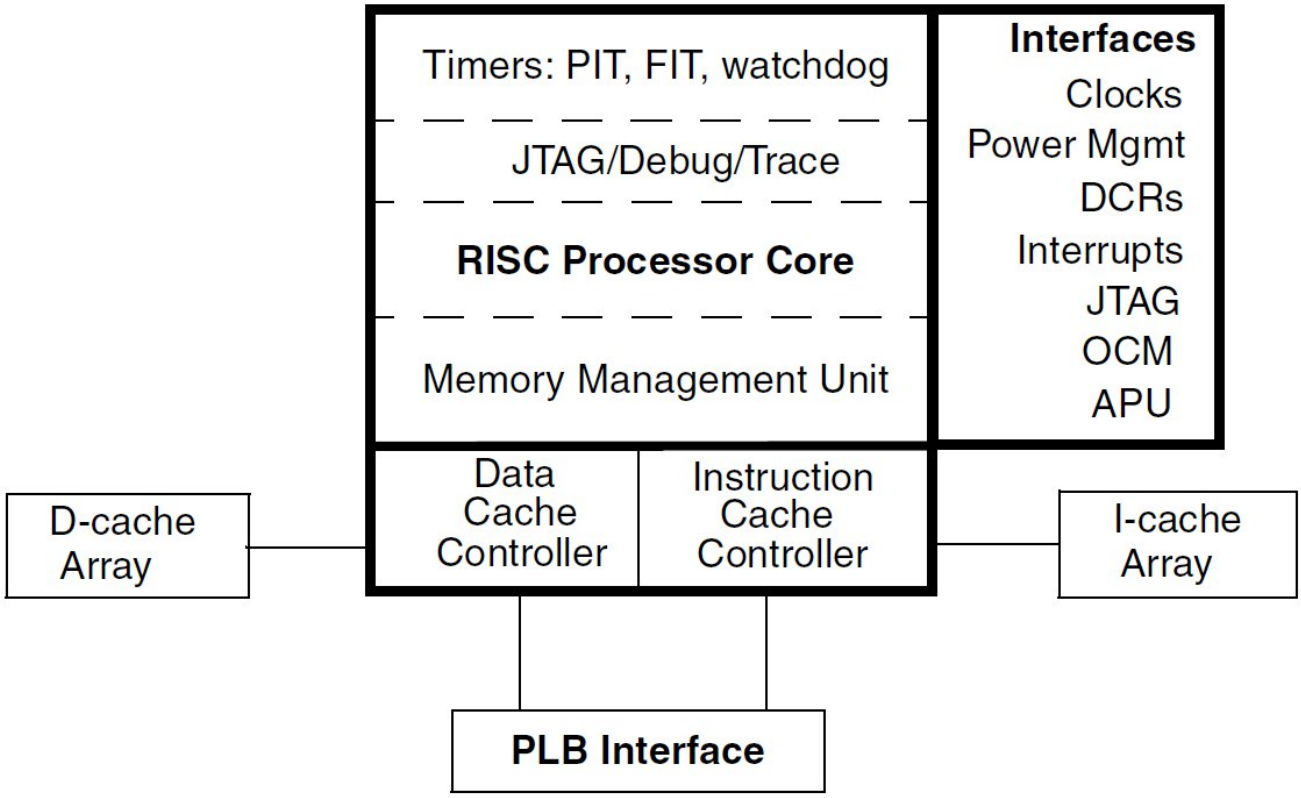
Version 1.0, November 2011

Introduction

The PPC405 provides a PowerPC core for applications which require PowerPC compatibility. It is a soft core and is not intended for high-performance applications. However, since it can be placed into any FPGA, it offers low power consumption. This makes it perfect for applications which require the use of a PowerPC and low power.

Features

- **PowerPC User Instruction Set Architecture (UISA) and extensions for embedded applications**
- **Thirty-two 32-bit general purpose registers**
- **Static branch prediction**
- **Five-stage pipeline with single-cycle execution of most instructions, including loads/stores**
- **Unaligned load/store support to cache arrays, main memory, and on-chip memory (OCM)**
- **Hardware multiply/divide for faster integer arithmetic (4-cycle multiply, 35-cycle divide)**
- **Multiply-accumulate instructions**
- **Enhanced string and multiple-word handling**
- **True little-endian operation**
- **Programmable interval timer, fixed interval timer, and watchdog timer**
- **Forward and reverse trace from a trigger event.**
- **Instruction and data cache units**
- **Memory Management translation of logical to physical addresses**
- **Support for OCM which provides memory access performance identical to cache hits**
- **Debug support**
- **Advanced power management support**



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Implementation Summary

Resource Utilization and Performance		
	Cyclone III	***Stratix III***
Logic	33K LEs	19K ALUTs
Registers	14K	13K
RAM	55 M9Ks	56 M9Ks
Speed	60 MHz	80 MHz
Supported Design Tools		
Altera	Quartus II 7.0 or later	

Customization

Octera can provide various peripherals and bridges, such as PLB-to-AHB, AHB-to-APB, memory controllers, etc.

Deliverables

- **Encrypted source code**
- **Fully synthesized FPGA**

Product code: OCT-405PPC

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